REMARKS

Claims 1, 5, and 9 were objected to because of informalities. The informalities have been corrected by the above amendments.

Claims 1-13 were rejected under 35 U.S.C. 103(a) as being unpatentable over Flanner in view of Blosse. The examiner in the response dated 9/10/02 states that in the Flanner et al patent the cap layer 6 is used as a hardmask and also that the antireflective layer 4 is used as a hardmask. As used in the instant invention the word hardmask is a term of art describing a layer that is used as a mask during an etch process. Observation of Figures 7-8 of the Flanner et al. patent show that it is the photoresist layer 2 that functions as the mask during the etch process. The photoresist layer 2 is present during the etch process and it is the photoresist layer 2 that masks the underlying layers and protects them during the etch process. Therefore it is the photoresist layer 2 that is used in the Flanner et al. patent as the mask and not the layers 4 and 6 as stated by the examine. Examiner of Figures 1(d) and 1(e) of the instant disclosure clearly show that layer 60 serves as the mask during the etch process and functions as a hardmask. The photoresist layer is not present during this etch process. Since this feature of the instant invention is not described or taught in either the Flanner at al. patent or the Blosse et al. patent then claims 1-13 cannot be rejected under 103(a) as being unpatentable over the Flanner et al patent in view of the Blosse et al. patent. The claims 1-13 are allowable over the cited art.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with Markings to Show Changes Made."**

To the extent necessary, Applicants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

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Version with Markings to Show Changes Made

In the claims:

1(Amended). A method for forming interconnects, comprising:

providing a silicon substrate containing one or more electronic devices;

forming a first dielectric layer over said silicon substrate;

forming a second dielectric layer over said first dielectric layer wherein the dielectric constant of the second dielectric layer is less [that] than 3.0;

forming a first hardmask layer over said second dielectric layer;

forming a second hardmask layer on said first hardmask layer wherein said second hardmask layer comprises a material selected from the group consisting of titanium aluminide (TiAl), titanium aluminum nitride (TiAlN), titanium nitride (TiN), aluminum nitride (AlN), tantalum aluminide (TaAl), and tantalum aluminum nitride (TaAlN);

forming a trench in said second dielectric; and

filling said trench with a conducting material.

5 (Amended). A method for forming interconnects, comprising:

providing a silicon substrate containing one or more electronic devices;

forming a first dielectric layer over said silicon substrate;

forming a second dielectric layer over said first dielectric layer wherein the dielectric constant of the second dielectric layer is less [that] than 3.0;

forming a first hardmask layer over said second dielectric layer;

forming a second hardmask layer on said first hardmask layer wherein said second hardmask layer comprises a material selected from the group consisting of titanium aluminide (TiAl), titanium aluminum nitride (TiAlN), titanium nitride (TiN), aluminum nitride (AlN), tantalum aluminide (TaAl), and tantalum aluminum nitride (TaAlN);

etching a first opening in said second hardmask layer of a first width;

forming a first trench of a second width in said second dielectric layer wherein said second width is less than said first width;

etching a second opening in said first hardmask layer of a first width;

forming a second trench of a first width in said second dielectric layer wherein said second trench is positioned over said first trench; and

filling said first and second [trench] trenches with a conducting material.

9 (Amended). A method for forming interconnects, comprising:

providing a silicon substrate containing one or more electronic devices;

forming a first etch stop layer over said silicon substrate;

forming a first dielectric layer over said first etch stop layer wherein the dielectric constant of the first dielectric layer is less than 3.0;

forming a second etch stop layer over said first dielectric layer;

forming a second dielectric layer over said [first] second etch stop layer wherein the dielectric constant of the second dielectric layer is less [that] than 3.0;

forming a first hardmask layer over said second dielectric layer;

forming a second hardmask layer on said [second] first hardmask layer wherein said second hardmask layer comprises a material selected from the group consisting of titanium aluminide (TiAl), titanium aluminum nitride (TiAlN), titanium nitride (TiN), aluminum nitride (AlN), tantalum aluminide (TaAl), and tantalum aluminum nitride (TaAlN);

etching a first opening in said second hardmask layer of a first width;

forming a first trench of a second width in said second dielectric layer wherein said second width is less than said first width;

etching a second opening in said first hardmask layer of a first width;

forming a second trench of a first width in said second dielectric layer wherein said second trench is positioned over said first trench;

simultaneously etching said second trench to a depth of said second etch stop layer and said first trench to a depth of said first etch stop layer; and

filling said first and second [trench] trenches with a conducting material.